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Switching Investigations on a SiC MOSFET in a TO-247 Package

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***Abstract*—This paper deals with the switching behavior of a SiC MOSFET in a TO-247 package. Based on simulations, critical parasitic inductances in the circuit layout are analyzed and their effect on the switching losses highlighted. Especially the common source inductance, a critical parameter in a TO-247 package, has a major influence on the switching energy. Crucial design guidelines for an improved double pulse test circuit are introduced which are used for practical investigations on the switching behavior. Switching energies of a SiC MOSFET in a TO-247 package is measured depending on varying gate resistance and loop inductances. With total switching energy of 340.24 µJ, the SiC MOSFET has more than six times lower switching losses than a regular Si IGBT. Implementing the SiC switches in a 3 kW T-Type inverter topology, efficiency improvements of 0.8 % are achieved and maximum efficiency of 97.7 % is reached.**

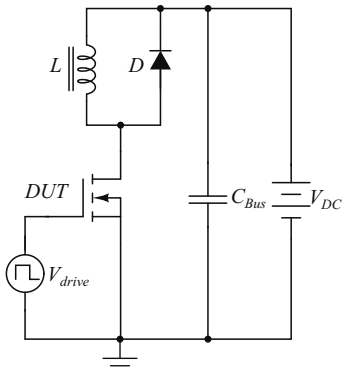
***Keywords*—SiC MOSFET, IGBT, multilevel inverter, Switching Energy**

I. Introduction

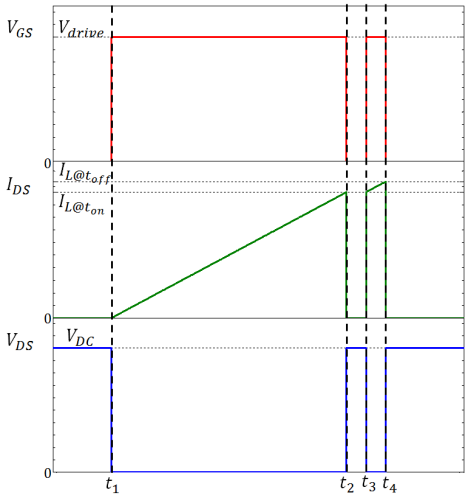
Silicon Carbide (SiC) devices have become more and more attractive in recent years by introducing SiC diodes which reduce stress on the main switching device due to the absence of reverse recovery current compared to Si diodes. One more way to increase efficiency in power converters is to replace Si switches by SiC switches such as SiC MOSFETs, SiC JFETs or SiC IGBTs. Their faster switching transitions compared to their Si counterparts enable possibilities to operate power converters at a high power density. Previous research has been done to investigate and utilize such devices in power converters in various applications [1]–[5]. Having fast switching transitions, a low parasitic printed circuit board (PCB) becomes more important. The purpose of this paper is to investigate the effect of parasitic elements in the circuit layout. Based on simulations, the influence of the PCB parasitic inductances on the switching energies is pointed out. A commonly used switching cell and PCB layout considerations optimized for fast switching transitions are introduced in order to limit such parasitic elements. Finally, on an optimized double pulse test (DPT) circuit, measurements on a SiC MOSFET in a TO-247 package are conducted in which switching energies are investigated relative to the gate resistance, the common source inductance as well as the junction capacitance of the freewheeling diode. Furthermore, the switching energies are compared to a Si IGBT. In Section II critical parasitic elements in a PCB circuit are investigated followed by a design guideline for PCB layouts with fast switching devices. The gate driver in the experimental setup is introduced in Section III. In Section IV, measurements on Cree's C2M0080120D SiC MOSFET are done showing switching behavior under different scenarios, e.g. varying gate resistance and stray inductance. Efficiency comparison of Si IGBTs and SiC MOSFETs in a 3 kW T-Type inverter are done in Section V. The conclusion is given in Section VI.

II. Double Pulse Tester

As the devices speed increase due to the reduced die parasitic capacitances, the circuit and package parasitic become more crucial in achieving the devices real performance. In this work, a DPT has been used for dynamic characterization. The double pulse tester is basically an inductor with a freewheeling diode that is used to evaluate the device under test (DUT) switching performance under clamped inductive load operation. The schematic of this circuit and the operating principle are shown in Fig. 1. At the instant t_1 the DUT is turned on and the inductor is charged up to the desired current level. At t_2 the DUT is turned off and the inductor current freewheels in the diode. At t_3 the DUT is turned on again and the turn on energy loss is measured by integrating the power in the switching interval. Finally the turn off energy loss is measured at the t_4 instant. The pattern is repeated for different current levels with a very low frequency repetition interval. In this way no self-heating effects are present and the characterization can be performed under controlled junction temperature conditions. The implemented prototype needs to offer flexibility and a modular design is preferred where different gate drive circuits can be tested by using a fast connection. The design is based on the digital signal processor (DSP) evaluation board C2000 Piccolo Launchpad. The implemented prototype is designed to accommodate a TO-247 for the switch and a TO-220 package for the diode. In order to extract the maximum switching performance of the evaluated devices, the DPT PCB design needs to be optimized. A Spice based simulation is used to evaluate the PCB parasitics impact on the device switching performance. The simulation circuit is constructed using a 1200 V, 20 A SiC MOSFET model from Cree Semiconductor *CMF20120* in TO-247 package and a 1200 V, 20 A SiC diode model from Rohm Semiconductor in TO-220 package. The simulation is implemented adding some PCB parasitics on top of the parasitics included in the models. The DPT with the circuit parasitic components is shown in Fig. 2. The simulation conditions are inductor current $I_L = 20\,\mathrm{A}$, supply voltage $V_{DC} = 800\,\mathrm{V}$ and gate drive voltage $V_{drive} = -5\,\mathrm{V}$ to $20\,\mathrm{V}$. Several simulations are performed varying the PCB parasitic



(a) Double pulse tester schematic



(b) Double pulse tester switching pattern

Fig. 1. Double pulse test circuit for evaluating switching performance of semiconductor power switches

inductances from 0 nH to 40 nH. The simulated turn on and turn off energy loss as well as the voltage overshoot at the DUT turn off event versus different parasitic inductances effects are shown in Fig. 3. According to the simulations, the gate drive inductance L_G does not have a remarkable effect on

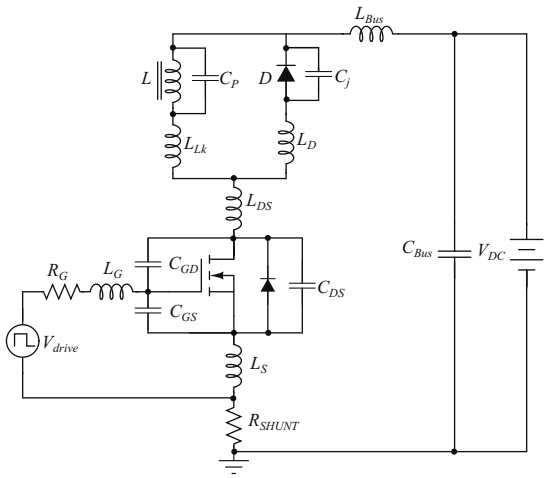
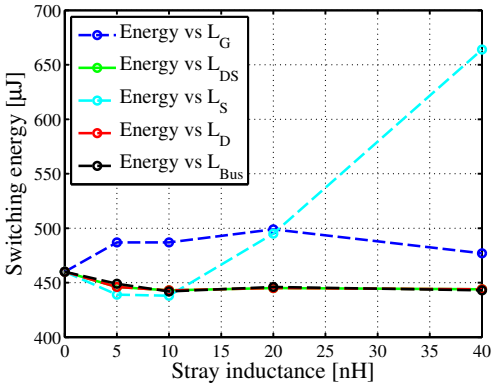
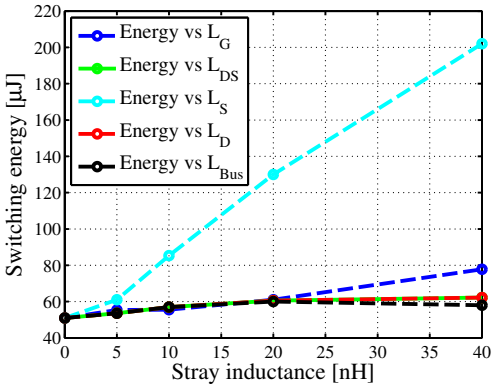


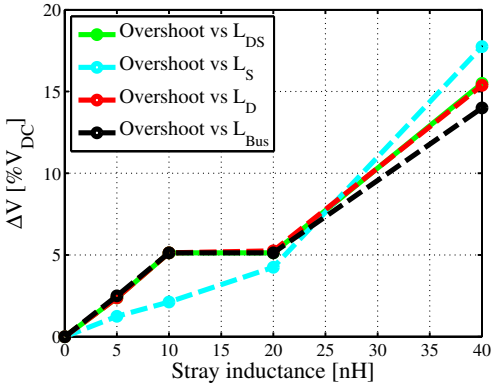
Fig. 2. Double pulse tester with parasitic components



(a) Simulated turn on energy loss vs. parasitic inductance



(b) Simulated turn off energy loss vs. parasitic inductance



(c) Simulated voltage overshoot vs. parasitic inductance

Fig. 3. Simulated switching energies and overshoot voltage on a non-ideal DPT

the device switching losses. During the turn on, the effect of this inductance will depend on the device threshold and the input gate charge. If these parameters are sufficiently large, the current through the driver loop parasitic inductance will build up before reaching the threshold voltage and the effect on the DUT switching energy will be minimal. The drain to source L_{DS} and diode L_D stray inductances do not increase the turn on loss and have a very small effect on the turn off energy loss that corresponds to the amount of stored energy on the stray fields when the DUT voltage reaches the supply voltage V_{DC}. In the same way, the supply loop stray inductance L_{Bus}

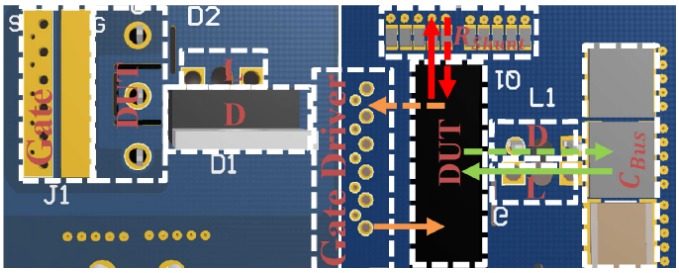


Fig. 4. DPT layout and current paths. Left (top view), right (bottom view)

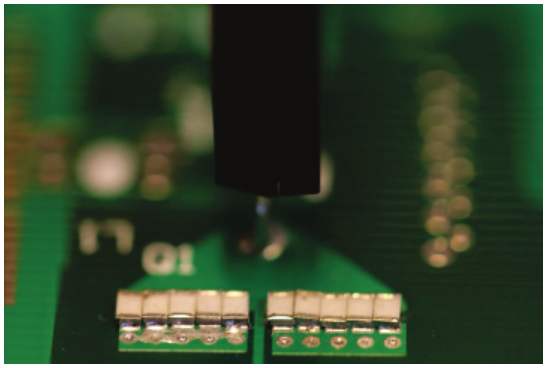


Fig. 5. Integrated flat current shunt

will slightly reduce the turn on loss because it will create a voltage drop across the DUT, and will increase the turn off energy loss in a similar way to the loop inductances L_{DS} and L_D. However, the common source inductance L_S affects considerably the DUT switching energy both at turn on and at turn off. This parasitic element, shared between the power and driver loops produces a negative feedback Eq. (1) in the gate control signal when a high derivative is present in the current flowing through the switch.

$$V_{GS} = V_{drive} \pm L_S \frac{dI_{DS}}{dt} \tag{1}$$

The double pulse tester needs to be designed trying to minimize all the parasitic inductances, paying special attention to the common source inductance. The gate drive inductance needs to be minimized too because a low impedance gate drive circuit helps reducing parasitc gate activation due to current injection into the gate trough the C_{GD} capacitance at turn off. The implemented prototype uses a four layer PCB to increase the degrees of freedom in the design. The critical loop areas are minimized by implementing the current return paths (the arrows in Fig. 4 indicate the different current loops) in a contiguous layer. Capacitive coupling between drain to gate and gate to source is avoided and the capacitance of the switching node is minimized to avoid increasing the dissipated energy at turn on. Finally, the common source inductance effect due to the PCB is avoided by keeping the power loop current (green and red arrows) orthogonal to the driver loop current (orange arrows). The current measurement method selection is based on a study of state of the art techniques. Recent research work based on characterization of fast switching devices use coaxial current shunts [6]. These devices claim bandwidths up to 2 GHz and are very suitable for this work due to the fact that they only introduce 2 nH in the switching loop. In order to further reduce the inserted stray inductance in the loop, the current measurement proposed in [7] is implemented in this work. This current measurement technique has been previously used for characterizing high switching speed [8] devices and represents a non intrusive and low cost solution. The current measurement bandwidth is increased by decoupling the measurement from the inductive effect of the resistive structure. This is performed by using a pick up wire placed strategically in a low field intensity region. Moreover, the inductance of the structure is further reduced by mounting the resistors upside down in order to place the resistive element closer to the PCB to minimize the area of the current loop. The implemented current shunt structure is shown in Fig. 5.

III. The Gate Driver

The gate driver used in this work comprises of a commercially available DC/DC converter, a digital isolator and a gate driver IC with a peak current capability of 9 A. The output of the DC/DC converter supplies ±15 V with a common ground on the secondary side. Two zener diodes are used to create the necessary voltage levels for the digital isolator as well as a reference voltage connected to the source terminal of the SiC MOSFET. An overview of the driver is shown in Fig. 6. With this constellation, the SiC MOSFET can be switched on with a positive voltage of 20.1 V and switched off with a negative voltage of −4.7 V.

IV. Practical Results

A. Low Side Measurements for Different Gate Resistances

Measurements on an optimized low side double pulse test circuit are conducted in order to investigate switching

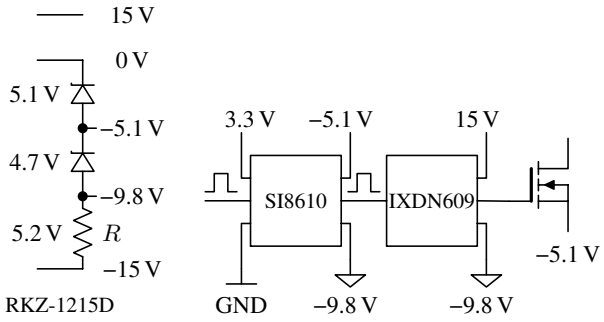


Fig. 6. Gate driver used for SiC MOSFETs

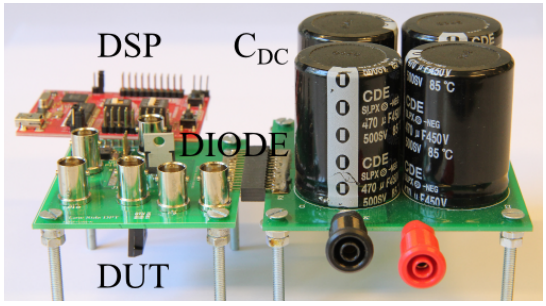
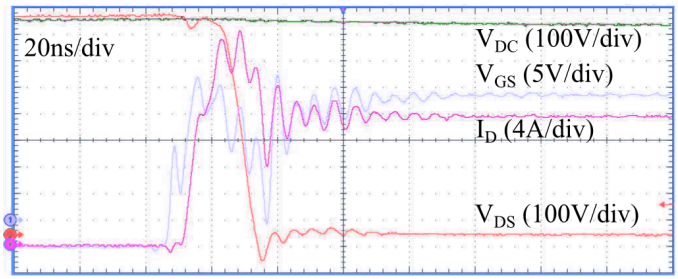
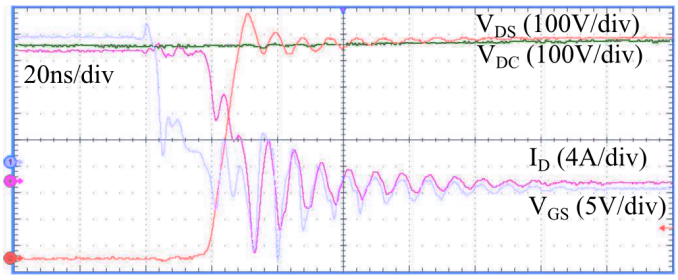


Fig. 7. Lab setup of the low side DPT



(a) Turn on transition



(b) Turn off transition

Fig. 8. Switching transition of a 1200 V SiC MOSFET in a double pulse test circuit. Gate resistance is 6 Ω

performance of SiC MOSFETs compared to varying gate resistors. The voltage probes in this work are Tektronix *P6139* (500 MHz) for the drain current and the gate to source voltage, and a Tektronix *P5100* (250 MHz) for the drain to source voltage. The DC link voltage is 800 V and the measured current range is from 5 A to 30 A. The setup can be seen in Fig. 7 and turn on and turn off transitions for a gate resistance of 6 Ω are shown in Fig. 8. Large oscillations in the gate to source voltage, the drain to source voltage as well as the drain current can be observed mainly due to the common source inductance of the TO-247 package. The resonance frequencies of the oscillations during turn on and turn off with SiC MOSFETs are 166.67 MHz and 125 MHz, respectively. The dv/dt for turn on and turn off are 84.6 V/ns and 85.88 V/ns. The di/dt is 8 A/ns and 1.33 A/ns for turn on and turn off, respectively. A common way to reduce and hence control the switching speeds is to increase the external gate resistance. The downside is an increase in switching energies due to the slower switching transitions. The switching energies for 0 Ω, 6 Ω and 12 Ω are

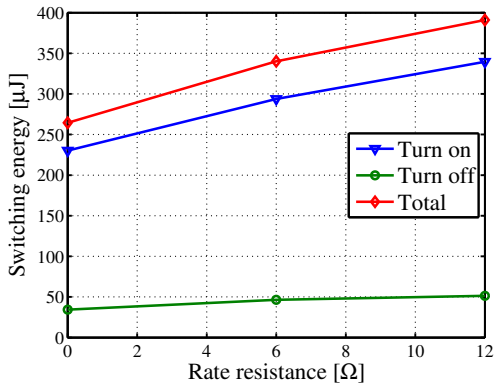
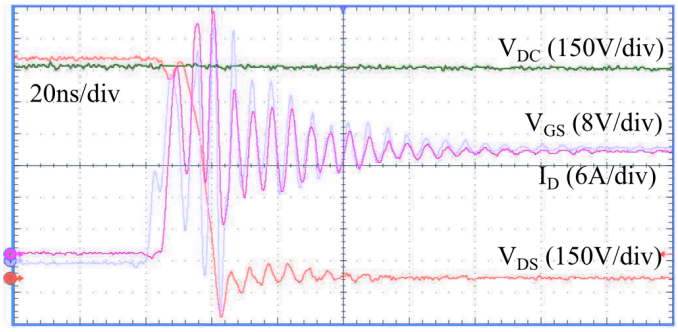
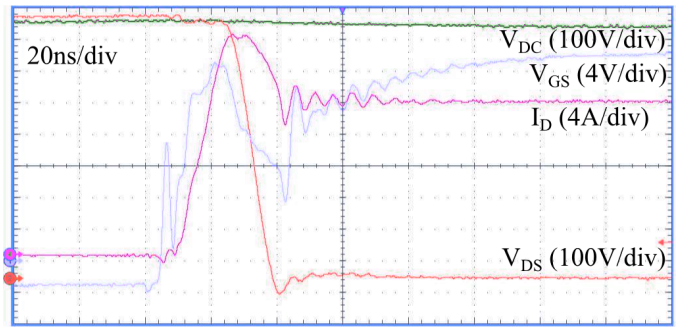


Fig. 9. Switching energies for different gate resistances



(a) Turn on transition for a gate resistance of 0 Ω



(b) Turn on transition for a gate resistance of 12 Ω

Fig. 10. Turn on transitions for different gate resistances

TABLE I. SEMICONDUCTOR COMPARISON

	$I_C/I_D[A]$	$Q_{Gate}[nC]$	$t_r[ns]$	$t_f[ns]$
IKW15N120T2	30	93	30	176
C2M0080120D	31.6	49.2	13.6	18.4

presented in Fig. 9. It can be seen that the turn on losses are mainly affected by an increased gate resistance whereas the turn off losses only slightly increase. A turn on switching comparison with 0 Ω and 12 Ω is shown in Fig. 10. Increasing the gate resistance reduces the peak gate current and hence the gate capacitance is charged slower such that the parasitics in the package as well as in the circuit become less critical. Especially the pointed out common source inductance shown in Eq. (1) has less influence.

B. *Comparison to a Si IGBT*

Commercially SiC switches come with a minimum breakdown voltage of 1200 V for different current ratings. Hence they are an alternative to replace 1200 V IGBTs in grid-tie applications, e.g. in photovoltaic systems, or motor drives. A comparison to a Si IGBT is conducted in order to see the reduction in switching energies. The chosen Si IGBT is Infineons IKW15N120T2, a second generation IGBT designed for frequency converters and uninterruptable power supplies. The main characteristics based on the semiconductor datasheets are listed in Table I. The same gate driver circuit as in Fig. 6 was used with the same voltage levels for turn on and turn off. Only the gate resistance was changed to 7 Ω in order to maintain the same peak gate current. The results can be seen in Fig. 11. Especially the turn off comparison shows the superior advantages of SiC MOSFETs over Si IGBTs due to the lack of the tail current. A total switching energy reduction of 84.2 % can be achieved at a switching current of 20 A.

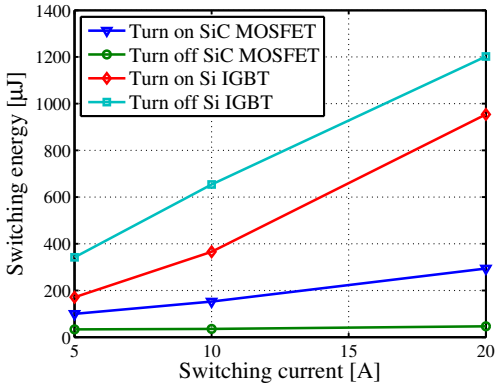
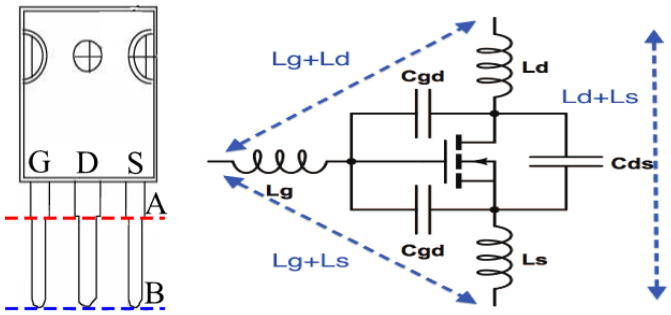


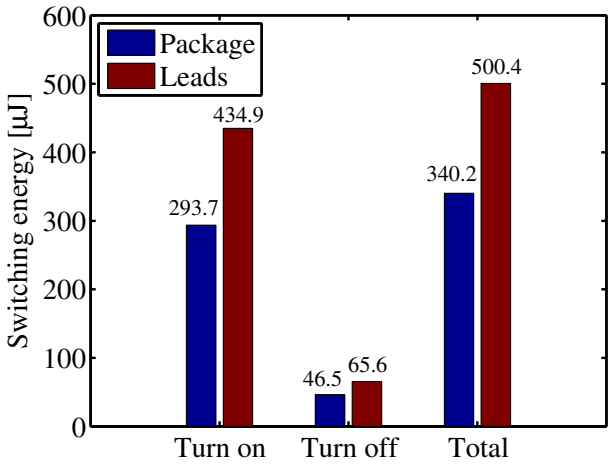
Fig. 11. Switching energy comparison between SiC MOSFET and Si IGBT

C. Effect of the lead inductance of the package

In the simulations, it is found out that the common-source inductance is a crucial aspect when it comes to switching energies. An increased inductance in the source path results in a larger switching energy loss. With an optimized PCB layout, the effect of the inductance of the leads of the TO-247 package is analyzed. A typical 1200 V switch in such package is shown in Fig. 12a and two kind of measurements were done. The first measurement represents the TO-247 SiC device being soldered to the DPT at the end of the leads (Point B, blue dotted line) from now on referred to as lifted leads. In the second measurement, the device is soldered to the DPT at the beginning of the leads (Point A, red dotted line). The comparison of these two scenarios with Cree's C2M0080120D SiC MOSFET is shown in Fig. 12b. It can be seen that having the TO-247 package soldered to the main PCB on Point A reduces the total switching energies by 32 %.



(a) Typical switch in a TO-247 package

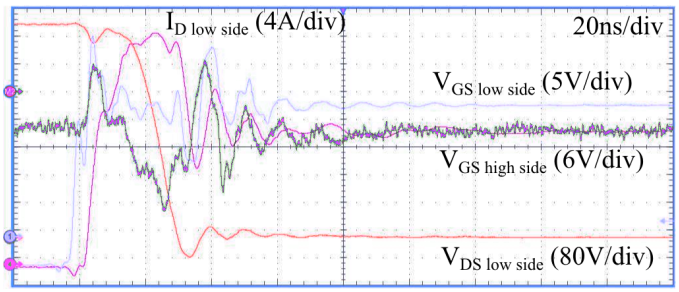


(b) Switching energies for different soldering points of the TO-247 package

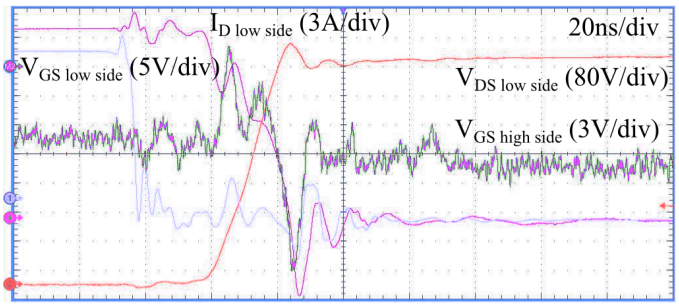
Fig. 12. Effect of the leads in a TO-247 package

D. Comparison of High Side Body Diode and Discrete SiC Diode

Until now, the DPT circuit comprised of a low side switch and a discrete SiC diode for free-wheeling the load current. A commonly encountered circuit configuration in power electronics is a phase leg comprising of a DC link voltage, a low side switch and a high side switch. Unlike Si IGBTs, SiC MOSFETs contain a parasitic body diode which can be used as a freewheeling diode. The effect of such body diode in the high side switch is investigated in this section and compared to a phase leg with an external SiC diode in parallel to the high side switch. Turn on and turn off transitions of the low side MOSFET as well as the gate to source voltage of the high side MOSFET are shown in Fig. 13. It can be seen that the gate to source voltage of the low side MOSFET is not dramatically affected by the switching transition. However, the gate to source voltage of the high side MOSFET is very much affected. By looking at the drain current through the low side MOSFET, it can be seen that no shoot through nor breakdown of the high side gate occurs. Comparing the switching energies of the low side MOSFET with a high side body diode and a discrete SiC diode, it can be seen that main efficiency improvements are achieved during the turn on process. At low current levels, the turn on energies using only the body diode presents the lowest losses because of the reduced parasitic capacitance. When an external SiC diode is used the increased



(a) Turn on transition



(b) Turn off transition

Fig. 13. Switching transition of a phase leg configuration

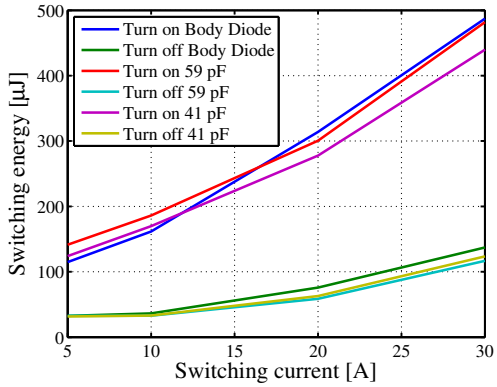


Fig. 14. Switching energies comparison for high side body diode and discrete SiC diodes

junction capacitance increases the losses at low current levels, however reduces the losses at high current levels because of the reduced reverse recovery effect in the body diode of the MOSFET. The turn off energies are less affected by the choice of discrete SiC diode or internal body diode as it can be seen in Fig. 14.

V. Efficiency Improvements Using SiC Switches

The effect of SiC switching devices is demonstrated on a 3 kW T-Type inverter whose schematic is shown in Fig. 15. It is a three level inverter topology that comprises of both 600 V and 1200 V semiconductor devices. More elaborated, switches S_3 and S_4 including their anti parallel diodes are 600 V devices because they have to withstand half the DC link voltage whereas S_1 and S_2 including their freewheeling diodes must be 1200 V devices because they have to block the whole DC link voltage. Furthermore, S_1 and S_2 are modulating the converter output voltage with a chosen switching frequency; typical values for residential photovoltaic applications are up to 20 kHz when Si IGBTs are used. The specifications are shown in Table II. A prototype of the T-Type inverter is designed according to the results and PCB guidelines in Section II in order to minimize the common-source inductance. Also, the switching devices are soldered to the PCB with a

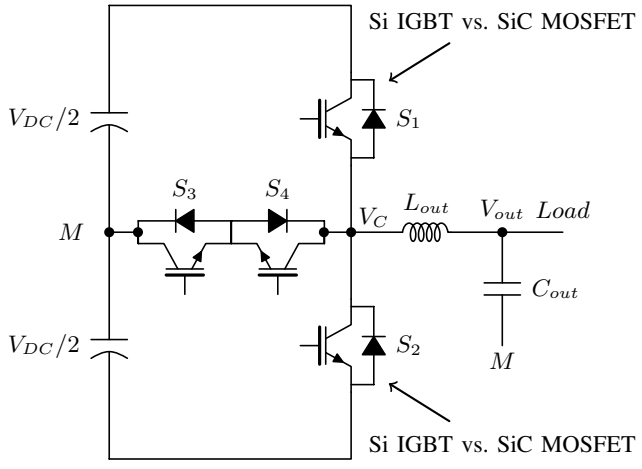
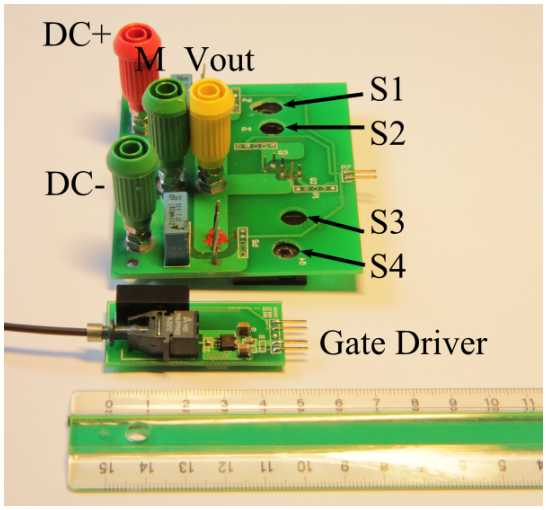


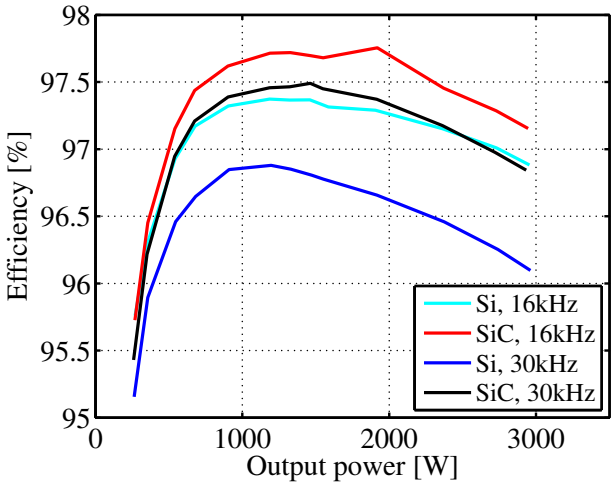
Fig. 15. T-Type inverter topology

TABLE II. Specifications

Symbol	Meaning	Value
L_{out}	Output filter inductance	3 mH
C_{out}	Output filter capacitance	4.4 µF
V_{DC}	DC link voltage	800 V
V_{out}	Filtered output voltage, RMS	230 V
P_{out}	Output power	250 W to 3000 W



(a) 3 kW prototype of T-Type inverter



(b) Efficiency improvements with SiC MOSFETs

Fig. 16. Prototype in (a) and measured efficiencies in (b)

minimum lead lengths (Point A in Fig. 12). The prototype as well as the efficiency curves using a N4L PPA5500 power analyzer for both the Si IGBT (IKW15N120T2) and the SiC MOSFET (C2M0080120D) version are shown in Fig. 16. Maximum efficiency improvements of 0.3 % are achieved at a switching frequency of 16 kHz. However, the benefits of the SiC switches become more visible as the switching frequency is increased up to 30 kHz. Maximum efficiency improvements at that switching frequency is then up to 0.8 %. According to the measurement results, the SiC based T-Type inverter at 30 kHz achieves similar efficiencies than the Si IGBT based inverter at 16 kHz.

VI. Conclusion

In this paper, switching performance of a commercially available SiC MOSFET has been investigated on a low parasitic DPT. Simulations have shown that the common source inductance has a significant negative impact on the switching losses. PCB design recommendations have been pointed out how to minimize such parasitic. In an optimized DPT circuit, a SiC MOSFET in a TO-247 package was evaluated based on different gate resistances. Even though the DPT is optimized for a low common source inductance, large oscillations are present due to the package parasitics. With a gate resistance of $6\,\Omega$ and a trade off between switching energy and oscillations, the SiC MOSFET has switching energies of 84.2 % lower than a Si IGBT. It is furthermore pointed out that the reverse recovery effect of the body diode of the high side MOSFET has a strong influence on the switching energies at higher current levels. Furthermore, it is recommended to use an external SiC diode with a low junction capacitance instead of using the body diode of the SiC MOSFET. Having SiC MOSFETs equipped in a 3 kW T-Type inverter, efficiencies could be increased by 0.8 % compared to a Si IGBTs counterpart.

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